

Towards pW-Class IoT Nodes Using Crystalline Oxide Semiconductor Dynamic Logic

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Abstract—Minimum operating power limits possible energy sources in IoT nodes. This paper considers dynamic logic circuits based on c-axis aligned crystalline indium-gallium-zinc-oxide FETs as a design style reducing the minimum operating power of digital systems. A method for ensuring timing and signal integrity and the integration into a standard-cell design flow is presented. Based on a generated logic library, a RISC-V CPU with an outstanding estimated minimum operating power of 6.0 pW is presented. This result shows that systems based on this logic family surpass comparable systems based on CMOS technologies in terms of minimum operating power.

I. INTRODUCTION

Physical dimensions, functionality and lifetime of smart Internet-of-Things (IoT) objects such as wireless sensor nodes are limited by power requirements and the need to integrate suitable power sources into products. At low operating frequencies, static leakage currents in silicon transistors dominate power consumption and limit the possible energy sources that a system can operate from.

Recent approaches to reduce static power consumption in silicon-based systems include dynamic leakage suppression (DLS) logic [1, 2] and feedforward leakage suppression logic [3], which managed to push leakage into sub-nW range. Further reduction in leakage remains ultimately limited by parasitic conduction in silicon FETs.

Oxide semiconductor field effect transistors (OSFETs) based on c-axis aligned crystalline indium-gallium-zinc-oxide (CAAC-IGZO) are considered as a complement and alternative to silicon FETs due to their exceptionally good off-state performance with leakage currents below 10^{-23} A/ μm [4]. OSFETs have previously been successfully employed in low-power display [5, 6], memory [7–9] and logic applications. In contrast to previously implemented normally-off low-power processors [10–12] that incorporate the OSFET as auxiliary device to aid state retention in designs that otherwise rely on silicon devices for computation, this paper addresses feasibility, design flow and power consumption of digital systems entirely based on OSFETs using OSFET dynamic logic (OSDL).

Section II introduces OSDL and includes a timing and signal integrity analysis. Section III presents a standard-cell based design flow for complex logic systems based on OSDL. In Section IV, the implementation of a RISC-V processor using OSDL and further system-level considerations are described. In Section V, simulation results are presented and compared

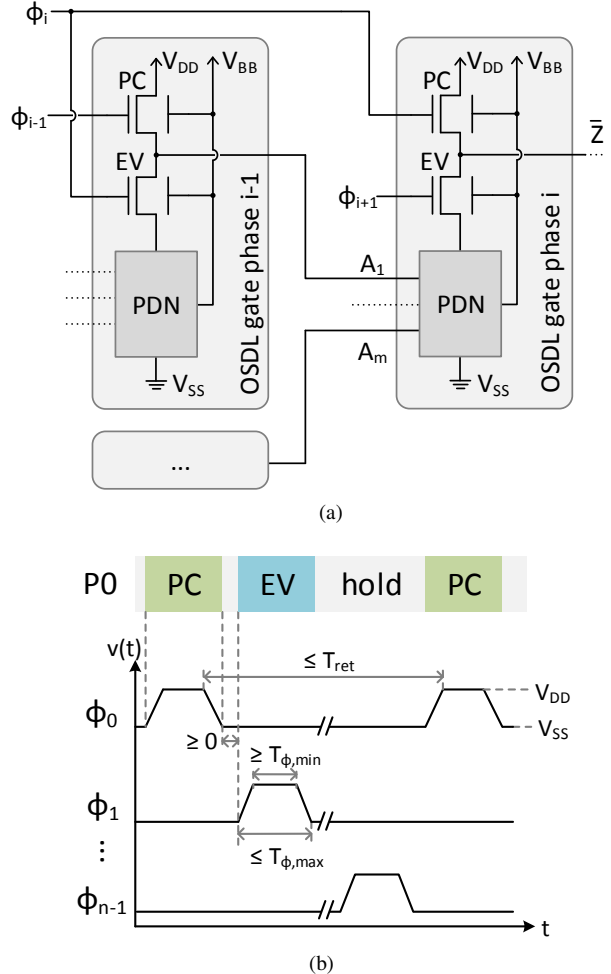


Fig. 1. OSDL logic family (a) and corresponding clocking schema (b). PC / EV mark precharge / evaluate transistors and corresponding clocking phases.

to previous work. The paper closes with a conclusion in Section VI.

II. OSFET DYNAMIC LOGIC

Because OSFETs are n-channel devices only, logic families such as CMOS that rely on complementary n- and p-channel devices cannot be realized without introducing leakage-prone silicon devices. Dynamic logic circuits do not require both n- and p-channel devices and therefore are the basis for OSDL. A

working shift register has previously been demonstrated using this design style [9].

Fig. 1a shows a circuit schema of OSDL. The presented OSDL gate consists of a precharge transistor (PC), an evaluate transistor (EV) and a pull-down network (PDN). The PDN can realize arbitrary negative unate boolean functions. To achieve a valid output signal, a positive clock pulse at the PC input has to be followed by a non-overlapping positive clock pulse at the EV input.

For clocking of PC and EV, a set of non-overlapping clocks $\phi_0, \dots, \phi_{n-1}$ is applied as depicted in Fig. 1b. Each logic gate is assigned to one logic phase i between 0 and $n-1$. The PC transistor is connected to clock ϕ_i and the EV transistor to clock ϕ_{i+1} . Hence, EV / PC clocks of gates assigned to adjacent phases are shared. Modulo n logic for clock indices is assumed.

The output \bar{Z} of a given logic gate of phase i is unconditionally precharged using the positive pulse of ϕ_i . The following positive pulse of ϕ_{i+1} then produces a valid output signal. Between the falling edge of ϕ_{i+1} and the following rising edge of ϕ_i , the output signal \bar{Z} is valid but not driven by any transistor. This phase is marked as *hold*. To ensure that input signals A_1, \dots, A_m are valid during the EV phase, they need to be driven by gates of neither phase i nor $i+1$.

A. OSFET Manufacturing and Device Model

OSFETs have been manufactured and characterized for different target applications. Simulations in this paper are based on characterization data from a recently published 21 nm long and 25 nm wide OSFET [4] with fin-style top-gate and independent back-gate.

Even though OSDL itself utilizes only n-channel OSFETs, auxiliary p-channel devices are desired for integration of a clock generator and helpful for peripheral memory and I/O circuits. For this purpose, OSFETs can be manufactured on top of a standard silicon CMOS process or possibly be combined with organic p-type transistors on top of an insulating substrate.

A compact device model has been implemented for analog SPICE circuit simulation that employs the following equation for drain current I_{ds} in the subthreshold region:

$$I_{ds} = \frac{W}{L} \cdot I_{d,0} \cdot e^{(V_{gs} + \chi V_{bs} - V_{th,0}) / (n \cdot V_T)} \cdot (1 - e^{-V_{ds} / V_T}), \quad (1)$$

where V_{gs} denotes the gate-source voltage, V_{bs} the back-gate-source voltage, V_{ds} the drain-source voltage and V_T the temperature voltage. Characteristics of $I_{d,0} = 8.4 \text{ nA}$, $\chi = 80 \text{ mV/V}$, $n = 1.51$, $V_{th,0} = 0.9 \text{ V}$ were used for the model.

B. Output Node Capacitance Model

Dynamic logic relies on the capacitances of each output net \bar{Z} for retention of logic states during the hold phase. For pre-layout estimation, output net capacitance $C_{\bar{Z}}$ due to input gate and interconnect is modeled as a function of fan-out (wire load model) and separated into two components $C_{\bar{Z}}(\text{FO}) = C_{\bar{Z},G}(\text{FO}) + C_{\bar{Z},C}(\text{FO})$, where $C_{\bar{Z},G}$ contains capacitances to V_{DD} , V_{SS} and V_{BB} that can be lumped to ground and $C_{\bar{Z},C}$

represents a coupling capacitance to other data signals that are possible crosstalk aggressors. Interconnect resistances are not modeled due to them being significantly lower than OSFET on-resistance.

To minimize signal degradation, the ratio of the capacitive divider $C_{\bar{Z},C} / C_{\bar{Z}}$ has to be kept small by shielding the output nets. We assume $\alpha = 0.9$ as the fraction of interconnect capacitance that contributes to $C_{\bar{Z},G}$. For our calculations we have conservatively modeled the interconnect with a capacitance of $0.2 \text{ fF}/\mu\text{m}$ and an approximate wire length of $7 \mu\text{m}/\text{FO}$, resulting in a per-fanout interconnect capacitance of $C_{IC/\text{FO}}$. For simplicity, we furthermore assume that each fan-out connection is to a maximum-sized gate input of capacitance $C_{g,\text{in}}$. $C_{d,\text{EV}}$ and $C_{s,\text{PC}}$ are capacitances seen from drain / source of the EV / PC transistors. A fixed per-cell storage capacitor C_{storage} is used to enhance retention and reduce the capacitive divider. The capacitances were consequently modeled as

$$C_{\bar{Z},G}(\text{FO}) = C_{s,\text{PC}} + C_{\text{storage}} + \text{FO} \cdot \alpha \cdot C_{IC/\text{FO}}, \quad (2)$$

$$C_{\bar{Z},C}(\text{FO}) = C_{d,\text{EV}} + \text{FO} \cdot ((1 - \alpha) \cdot C_{IC/\text{FO}} + C_{g,\text{in}}). \quad (3)$$

Due to an equivalent oxide thickness of 6 nm for the top gate, interconnect capacitances dominate $C_{\bar{Z}}$.

C. Timing / Signal Integrity Characterization

For correct operation, it needs to be ensured that output nodes are sufficiently discharged when a continuous PDN path has been turned on by high input signals (*switch-on test*), and that a PDN path with a low input signal does not cause degradation of a precharged output signal beyond an acceptable margin (*switch-off test*). Goal of this characterization is to determine whether reliable logic operation can be achieved at all, and to find a global fan-out limit to ensure reliable operation. Initial characterization is done at the worst-case hot design point ($T = 60^\circ\text{C}$), a supply voltage of $V_{DD} = 0.8 \text{ V}$, a given back-gate voltage $V_{BB} = 0 \text{ V}$ and a minimum clock pulse width of $T_{\phi,\text{min}} = 83 \text{ ms}$.

Local clock buffering of the clock phases is not required, since clock transition times are not a critical factor of OSDL timing and clock frequencies allow disregarding interconnect resistances.

Due to the asymmetry of using n-channel devices for both PC and EV, a complete discharge of output nodes corresponding to an output low voltage of $V_{OL} = V_{SS}$ is achieved, whereas the PC transistor turns itself off as output node voltage rises, resulting in a logarithmic precharge curve and a high output voltage of $V_{OH} < V_{DD}$ of a previously discharged output node. Fig. 2 shows typical signal behavior.

a) *Switch-on test*: The switch-on testbench is shown in Fig. 3. It contains a precharge test gate that produces an output voltage v_{PC} at an initially discharged $C_{\bar{Z}}(\text{FO})$ -sized capacitor for a given fan-out FO and a minimum-length precharge pulse ϕ_0 . Continuous PDN path inputs of a collection of evaluate test gates are connected to a voltage-dependent voltage source $v_{in}(v_{PC})$ which simulates degradation of the output voltage through the capacitive divider introduced in Section II-B and

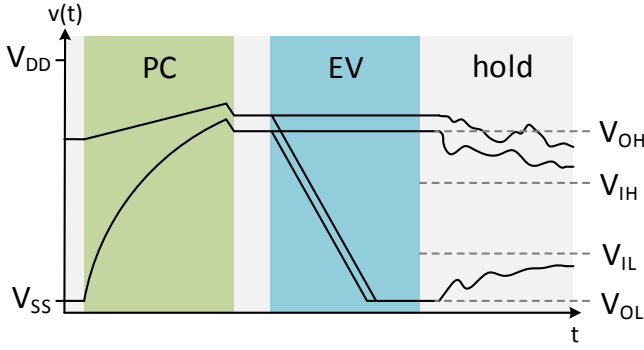


Fig. 2. Exemplary output signal waveforms for low-to-low, low-to-high, high-to-low and high-to-high transitions.

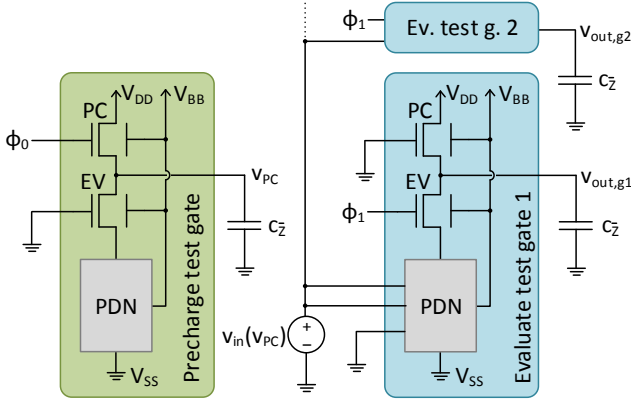


Fig. 3. Simulation setup for switch-on test.

pre-defined noise margins for hold and evaluate $V_{NM,hold} = 20 \text{ mV}$, $V_{NM,EV} = 50 \text{ mV}$:

$$v_{in}(v_{PC}) = \frac{C_{Z,G}(FO)}{C_Z(FO)} \cdot v_{in} - V_{NM,hold} - V_{NM,EV} \quad (4)$$

After the PC pulse, an equally long EV pulse at ϕ_1 causes discharging of the initially fully charged $C_Z(FO)$ -sized capacitors $v_{out,i}$. In the testbench, the voltages v_{PC} and $v_{out,i}$ are measured after the clock pulse ϕ_1 . The global fan-out limit is given by the highest FO that allows full discharging of all voltages $v_{out,i}$.

b) *Switch-off test*: Voltages at output node capacitors that have previously been fully discharged ($V_{OL} = V_{SS}$) during evaluation can also be degraded by the capacitive divider and $V_{NM,hold}$. The maximum low input voltage V_{IL} can thus be calculated. The worst-case pull-down current I_{IL} of a PDN driven by V_{IL} is found through DC simulation and leads to the maximum clock pulse width by which degradation does not exceed $V_{NM,EV}$:

$$V_{IL} = \frac{C_{Z,C}(FO)}{C_Z(FO)} \cdot V_{DD} + V_{NM,hold} \quad (5)$$

$$T_{\phi,max} = \frac{C_Z(1) \cdot V_{NM,EV}}{I_{IL}} \quad (6)$$

This shows that maximum clock pulse width depends on the minimum output capacitance. $C_{storage}$ can be used to ensure that $T_{\phi,max} > T_{\phi,min}$ and timing margins are sufficient.

D. Retention Time

During normal operation in the hold phase, OSDL output node voltages can be degraded by leakage currents through the EV and PC transistors. The current I_{off} through an EV transistor with $V_{gs} = 0 \text{ V}$ determines retention time T_{ret} as shown in Fig. 1b and the associated minimum operating frequency for always-on operation:

$$T_{ret} = \frac{C_Z(1) \cdot V_{NM,hold}}{I_{off}} \quad (7)$$

E. Back-Gate Temperature Compensation

It is desirable to keep I_{ds} temperature-invariant for a gate voltage between V_{IL} and V_{IH} . This can be achieved with dynamic V_{BB} biasing. The back-gate biasing proposed here keeps I_{IH} , the drain current corresponding to V_{IH} , temperature-invariant. This results in a constant $T_{\phi,min}$ and increasing $T_{\phi,max}$ and T_{ret} for decreasing temperatures.

III. STANDARD-CELL BASED DESIGN FLOW

A. OSDL Cell Library

A Liberty timing library, SPICE sub-circuits and functional Verilog views of an OSDL library with 51 gates were generated. Each gate implements a single-stage negative unate function such as INV, NOR2, NAND4, AOI333, OAI333. A 10-fin PC transistor, 1-fin EV transistor and 2- to 4-fin PDN transistors (depending on stacking) have been used. A per-cell storage capacitance $C_{storage}$ of 3 fF has been chosen.

The generated Liberty model associates a constant propagation time and the previously discussed library-wide maximum fan-out to all gates. The constant propagation time directs the timing-driven synthesis tool to minimize the number of logic stages.

B. Logic Synthesis

To enable RTL-to-netlist synthesis with conventional synthesis tools, a dummy flip-flop cell (DFF) has been added to the Liberty timing library. A typical single-clock, synchronous-reset RTL design is then translated into a netlist that contains both OSDL gates and DFFs, where the number of OSDL gates between DFFs is optimized.

This netlist is then transformed by a custom post-processing script into a functioning OSDL design using following steps:

- 1) Every OSDL gate is assigned to a clock phase i where i is the farthest distance in number of gates from its inputs to a DFF.
- 2) The number of clock phases n is set in accordance with the maximal i present in the design. n has to be at least four.
- 3) For each OSDL gate G 's inputs (and every design output port) that is directly connected to a DFF or a chain of DFFs:

TABLE I
PARAMETERS OF SIMULATED OSDL LOGIC FAMILY AND CPU CORE

	$T = -30^\circ\text{C}$	$T = 0^\circ\text{C}$	$T = 30^\circ\text{C}$	$T = 60^\circ\text{C}$
V_{BB}	1.515 V	1.01 V	0.505 V	0 V
I_{IH}	301 fA	302 fA	303 fA	304 fA
I_{IL}	35 aA	94 aA	210 aA	407 aA
I_{off}	0.2 aA	1.0 aA	3.4 aA	9.6 aA
$T_{\phi,\text{max}}$	999 ms	391 ms	184 ms	99 ms
T_{ret}	470 s	96.8 s	28.5 s	10.1 s
$P_{\text{min,avg}}$	0.36 pW	1.78 pW	6.0 pW	17.0 pW

- A set of valid (cycle, phase) tuples for the OSDL input signal is determined based on G's phase.
- The (cycle, phase) tuple for the OSDL gate J at the DFF (chain) input is given by J's phase and the number of DFFs between J and G.
- Buffers (INV pairs) are inserted between J and G until the (cycle, phase) tuple of the final buffer output is within the set of valid (cycle, phase) tuples. If possible, existing buffers are reused.
- The possibly buffered output of J now replaces the DFF as driver of G's input.

4) All DFFs are removed from the netlist.

IV. RISC-V PROCESSOR AND SYSTEM INTEGRATION

The open-source PicoRV32 RISC-V CPU core [13] was synthesized in RV32I two-cycle-ALU configuration using the described standard-cell based OSDL design flow.

An integrated circuit suitable for pW-class IoT nodes would likely include an on-chip energy harvester, an ultra-low-power clock generator, memory and I/O alongside the OSDL CPU core. CMOS oscillators based on DLS logic, such as [14], are possible candidates for clock generation, as they function within the desired pW-level power budget. For main memory, a dynamic RAM based on OSFETs requiring no periodic refresh (DOSRAM) [7–9] could be utilized. To save power, the working registers of the OSDL CPU, which are currently realized using OSDL gates and therefore periodically refreshed, could also be implemented as DOSRAM.

V. SIMULATION RESULTS

The results of the switch-on test using $T_{\phi,\text{min}} = 83$ ms for five OSDL gates are shown in Fig. 4. Based on those results, the global fan-out limit was set to 13. Resulting worst-case levels are $V_{\text{OH}} = 631$ mV and $V_{\text{IH}} = 449$ mV. The switch-off test using a calculated $V_{\text{IL}} = 179$ mV leads to a maximum clock pulse width $T_{\phi,\text{max}} = 146$ ms at 60°C .

Temperature-dependent timing parameters using the dynamic- V_{BB} temperature compensation scheme from Section II-E are shown in Table I.

The resulting RISC-V CPU core utilizes 12 clock phases and consists of 11736 gates with a total transistor width of $4520\ \mu\text{m}$. The maximum clock frequency is 1 Hz. A test program was executed using gate-level digital simulation and an internal energy consumption of 62.8 pJ/cycle was found.

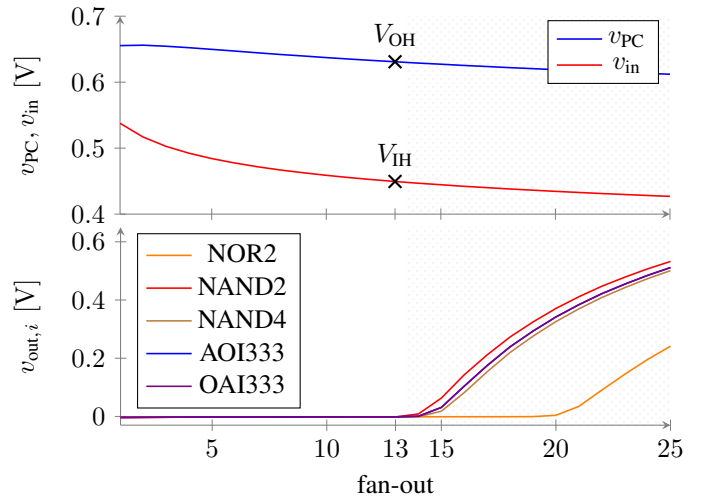


Fig. 4. Switch-on test simulation results.

TABLE II
COMPARISON OF OSDL CPU WITH OTHER LOW-LEAKAGE CPUS

	Proposed OSDL CPU	ISSCC '18 [2]	VLSP'17 [15]	ISSCC '15 [1]
Technology	21 nm CAAC-IGZO	180 nm Si	65 nm Si	180 nm Si
Type	pre-layout estimation	measurement results	measurement results	measurement results
Architecture	PicoRV32 (RV32I)	MSP430-compatible	ARM Cortex-M0+	ARM Cortex-M0+
Clock gen.	not impl.	included	excluded*	included
Freq. range	0.035–1 Hz	1 Hz–2.8 MHz	12 kHz–60 MHz	2–15 Hz
Min. power	6.0 pW	595 pW	46 nW	295 pW
Min. energy per cycle	171.5 pJ	14 pJ	6.3 pJ	44.7 pJ
Memory	not impl.	2 KB	12 KB	128 B
Supply volt.	0.9 V	0.2–1.1 V	0.29–1.2 V	0.16–1.15 V

*Implemented clock generator is excluded to improve comparability.

An additional energy of 108.7 pJ/cycle was calculated for charging and discharging of the clock nets based on the wire load model, leading to a total of 171.5 pJ/cycle. The minimum average operating power values $P_{\text{min,avg}}$ at retention speed are shown in Table I. A peak power requirement of 35 pW was found using transient simulation for the highest-load-phase ϕ_0 and an optimized 184 ms wide clock pulse.

Table II compares the proposed OSDL CPU with state-of-the-art conventional [15] and DLS CPUs [1, 2].

VI. CONCLUSION

In this paper, we introduced a method for ensuring timing and signal integrity of OSDL circuits and a standard-cell based design flow that can be used to easily port existing designs to crystalline oxide semiconductor technology. Using an OSDL implementation of an open-source RISC-V core, it has been revealed that the use of OSDL can drastically reduce minimum operating power of systems. This enables the design of IoT nodes powered by pW-level on-chip energy harvesting sources.

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